

KTM5300

21-bit High Resolution, High Accuracy Off-Axis
Magnetic Angle Encoder IC
Programmable ABZ/UVW/PWM/SPI Multi-Mode
Output Angle Sensor

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Revision History

Version	Date	Description
V1.0	2026-06	Initial release

Features

- Based on vertical Hall element technology; 0~360° absolute angular position sensing
- Supports off-axis installation: uses vertical Hall elements to sense the magnetic field component perpendicular to the chip surface, enabling accurate angle measurement in off-axis configurations
- 21-bit core angular resolution; supports speeds up to 60,000 RPM
- Angular output latency 2 μ s~10 μ s
- Closed-loop one-click self-calibration: INL reaches $\pm 0.03^\circ$ after off-axis calibration
- Supports non-uniform-speed self-calibration: optimizes calibration performance under non-constant speed conditions
- Operates over -40~125°C temperature range
- Simultaneous incremental ABZ, incremental UVW, PWM absolute value, and 4-wire SPI output
- ABZ incremental output: 1~65,536 pulses per revolution, any integer resolution, customer-programmable
- UVW incremental output: 1~64 pole pairs per revolution, any integer pole pair count, customer-programmable
- Built-in EEPROM; parameter programming and storage supported at 3.3 V~5.0 V supply
- QFN16L-3 $\times$ 3 package, suitable for off-axis installation

Applications

- Absolute angular position sensors
- Brushless DC motor control
- Servo motor control
- Closed-loop stepper motor control
- Replacement of optical encoders
- Off-axis mounting applications requiring compact magnetic assembly

Product Overview

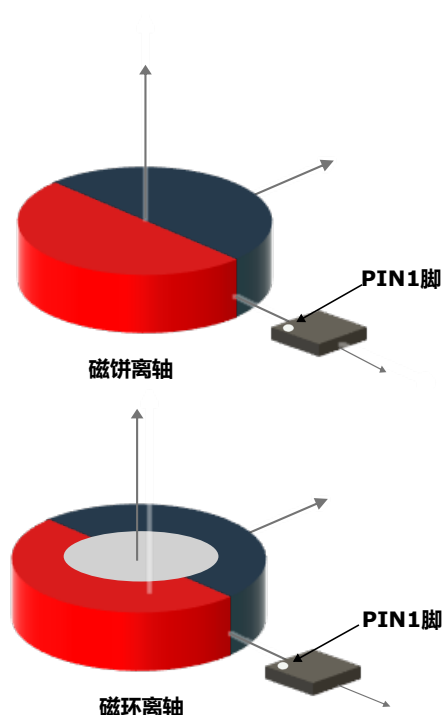


Figure 1: Off-Axis Magnetic Installation Overview

KTM5300 is a high-speed, high-accuracy angle encoder IC designed for off-axis mounting. Unlike on-axis AMR sensors, KTM5300 uses vertical Hall elements and dedicated signal processing to sense the magnetic field component perpendicular to the chip surface, allowing the magnet to be mounted beside (rather than above) the IC. This off-axis configuration simplifies mechanical integration in space-constrained designs.

KTM5300 uses an off-axis mounting configuration in a QFN16L-3×3 package; after calibration, INL accuracy can reach $\pm 0.03^\circ$ (typical), with temperature drift $\pm 0.5^\circ$ (typical).

KTM5300 provides an incremental ABZ output interface as a replacement for conventional optical encoders, with resolution up to 65,536 pulses per revolution (262,144 steps per revolution). Incremental UVW outputs support 1–64 pole pairs per revolution.

KTM5300 provides a 4-wire SPI interface for the host or MCU to read the chip's internal 21-bit absolute angle data, and supports single-wire PWM output of absolute angle data. Its core advantage is user-side one-click self-calibration, which compensates for nonlinear errors introduced by imperfect magnets and mounting offsets,

significantly improving INL performance.

1 Pin Definitions

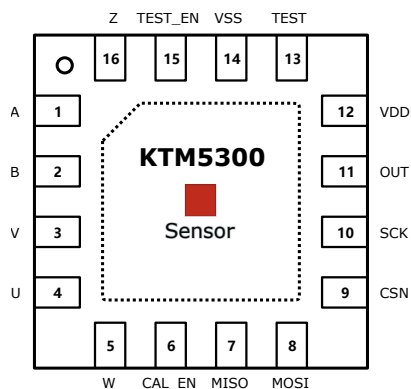


Figure 2: KTM5300 QFN3X3 Package Outline

Table 1: Pin List

Pin Name	No.	Pin Type	Description
A	1	Digital Output	Incremental A signal output
B	2	Digital Output	Incremental B signal output
V	3	Digital Output	Incremental V signal or –B signal output
U	4	Digital Output	Incremental U signal or –A signal output
W	5	Digital Output	Incremental W signal or –Z signal output
CAL_EN	6	Digital Input	Customer-side self-calibration enable control pin
MISO	7	Digital Output	SPI data bus; KTM5300 upstream data output
MOSI	8	Digital Input	SPI data bus; KTM5300 input data receive
CSN	9	Digital Input	SPI chip-select enable pin
SCK	10	Digital Input	SPI clock
OUT	11	Digital Output	PWM output
VDD	12	Power	3.3~5.0 V supply
TEST	13	Analog Input	Factory test pin (for CONNTEK use only)
VSS	14	Ground	Ground
TEST_EN	15	Digital Input	Factory test enable pin (for CONNTEK use only)
Z	16	Digital Output	Incremental Z signal output

2 Functional Block Diagram

KTM5300 is an angle sensor based on vertical Hall elements and dedicated signal-processing technology; it senses the magnetic field component perpendicular to the chip surface and outputs an angle value. As shown in the figure, the chip integrates vertical Hall sensing elements that output sinusoidal and cosinusoidal analog signals. The signals are amplified (G) and filtered by the analog front end, then digitized by the ADC; the DSP performs compensation, calibration, and angle computation. The final absolute angle can be output via SPI or PWM and further synthesized into incremental ABZ and UVW signals. The system also integrates an LDO, oscillator, and EEPROM.

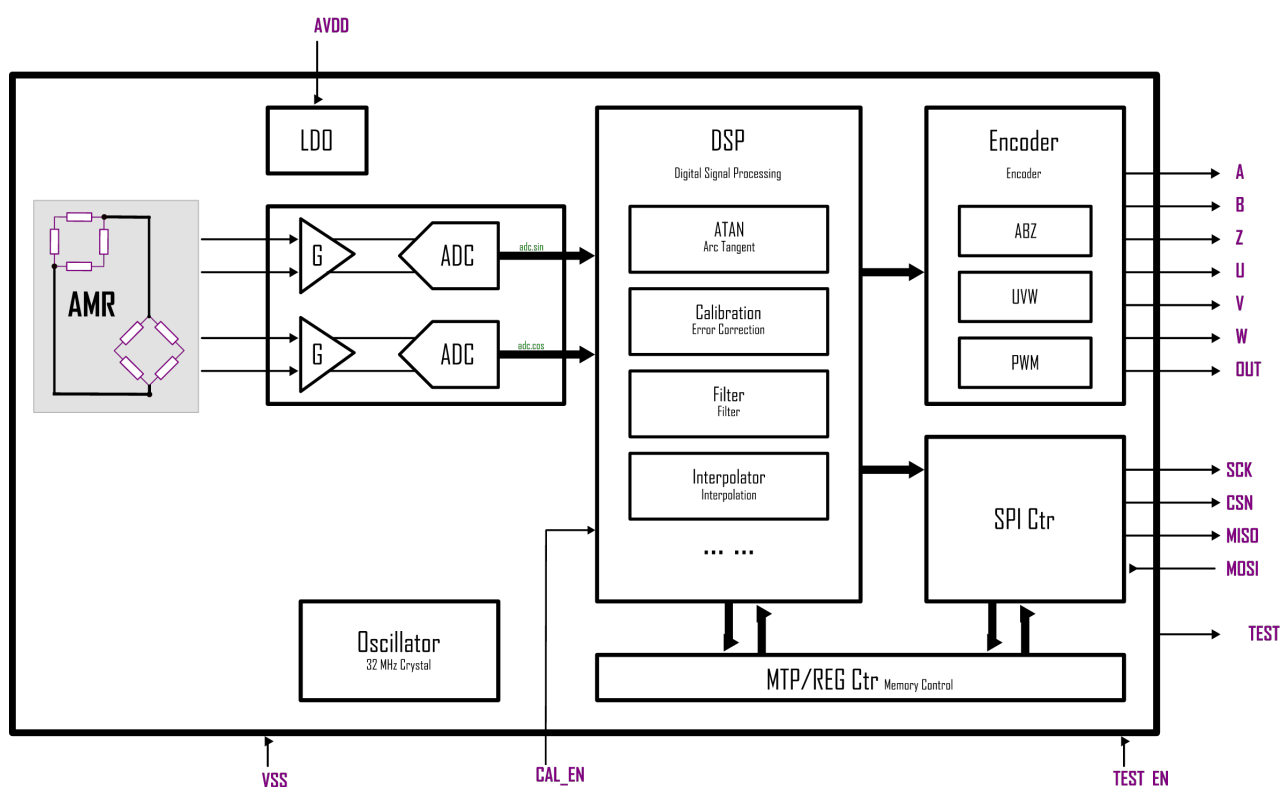


Figure 3: Chip Functional Block Diagram

3 Absolute Maximum Ratings

The following parameters represent the limit conditions the chip can withstand and do not represent the normal operating range. Exceeding the “Absolute Maximum Ratings” may cause permanent damage to the chip.

Table 2: Absolute Maximum Ratings

Parameter	Min	Max	Unit	Remarks
Supply Voltage	-0.5	6.5	V	
Pin Input Voltage Range	-0.5	VDD	V	ABZ, UVW, MISO , MOSI , SCK , CSN , TEST_EN , OUT , CAL_EN , TEST pins
Pin Output Current	-20	20	mA	ABZ, UVW, OUT , MISO pins
Storage Temperature	-40	150	°C	
Latch-up Immunity (Input Current)	—	±100	mA	Ref. AEC-Q100-004
ESD Immunity (Human Body Model)	—	±8.0	kV	Ref. AEC-Q100-002
ESD Immunity (Charged Device Model)	—	±1.5	kV	Ref. AEC-Q100-011

4 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Min	Max	Unit	Remarks
Supply Voltage	3.0	5.5	V	
Magnetic Field Strength	30	1,000	mT	
Speed	—	60,000	RPM	
Operating Temperature	-40	125	°C	

5 Electrical Characteristics

Unless otherwise specified, the following parameters are defined at supply voltage 4.5~5.5 V and temperature -40~125°C.

Table 4: Electrical Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
VDD	Supply Voltage	—	3.0	3.3~5.0	5.5	V
Idd	Operating Current	—	15	25	28	mA
LSB	Minimum Resolution (ABZ Mode)	N steps/rev	—	360°/N	—	°
INL	Integral Nonlinearity (off-axis, after calibration)	Note [1]	—	±0.03	—	°
DNL	Differential Nonlinearity	@ 2,500 pulses ABZ	—	±0.005	—	°
TN	Transient Noise (ABZ Mode)	@ 25°C; BW = 5	—	0.0015	—	°rms
Hyst	Hysteresis Window	Programmable	—	0.011	—	°
TPwrUp	System Power-up Ready Time	Supply ramp-up < 100 µs	—	64	—	ms
TDelay	System Latency	Constant speed	—	10	—	µs
TST	Step Response Time	BW = 5	—	100	—	µs
TEMP	Temperature Drift (off-axis)	-40~125°C	—	±0.5	—	°

Note [1]: Typical value measured at 25°C with zero eccentricity between magnet and chip; maximum value measured over full temperature range -40~125°C at maximum allowable air gap (AG) and maximum allowable eccentricity (DISP).

5.1 ABZ Output Parameters

Unless otherwise specified, the following parameters are defined at supply voltage 4.5~5.5 V and temperature -40~125°C.

Table 5: ABZ Output Parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
ABRES	AB Resolution	Programmable	1	—	65,536	lines/rev
ABFreq	A or B Frequency	Note (3)	—	—	8.192	MHz

Note (3): The AB output frequency ABFreq equals the product of speed RS and AB resolution ABRES. When AB resolution is configured to the maximum 65,536 lines/revolution, the maximum supported speed is:

$$RS_{MAX} = \frac{AB_{Freq}}{AB_{Res}} = \frac{8.192 \text{ MHz}}{65,536} = 125 \text{ Hz} = 7,500 \text{ RPM}$$

The AB output frequency limit of KTM5300 is configured by ABZ_LIMIT[1:0], with a maximum of 8.192 MHz.

5.2 PWM Output Parameters

Unless otherwise specified, the following parameters are defined at supply voltage 4.5~5.5 V and temperature -40~125°C.

Table 6: PWM Output Parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
FPWM	PWM Frequency	Programmable	-8%	497 or 994	+8%	Hz
TRise	Rise Time	Load CL = 1 nF	—	—	1	μs
TFall	Fall Time	Load CL = 1 nF	—	—	1	μs

5.3 Filter and Hysteresis Parameters

Filter and hysteresis behavior are primarily controlled by FILTER[7:0] and HYST[7:0]. HYST[7:0] can be converted to actual hysteresis angle by the formula:

$$\theta_{hyst}(^{\circ}) = \text{HYST}[7:0] \times \frac{360}{2^{18}}$$

The conversion resolution is approximately 0.001373°/LSB; at HYST = 255, the maximum hysteresis is approximately 0.349°.

Table 7: HYST[7:0] vs. Hysteresis Angle

HYST	Hysteresis (°)	HYST	Hysteresis (°)
0	0.000	100	0.137
1	0.001	200	0.274
10	0.014	255	0.349
50	0.069		

5.4 EEPROM Electrical Characteristics

Unless otherwise specified, the following parameters are defined at supply voltage 4.5~5.5 V and temperature -40~125°C.

Table 8: EEPROM Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
VDD	Supply voltage during erase/write and read	3.0	—	5.5	V
Endurance	Erase/write cycles	1,000	—	—	cycles
Retention	Data retention (@ 150°C)	10	—	—	years

5.5 General Digital I/O Characteristics

Unless otherwise specified, the following parameters are defined at supply voltage 4.5~5.5 V and temperature -40~125°C.

Table 9: General Digital I/O Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
VIH	Digital I/O input logic high (CSN , MOSI , SCK , CAL_EN)	—	$0.8 \times VDD$	—	—	V
VIL	Digital I/O input logic low (CSN , MOSI , SCK , CAL_EN)	—	—	—	$0.2 \times VDD$	V
VOH	Digital I/O output logic high (ABZ , UVW , MISO , OUT)	Push-pull (@ Iout = -2 mA)	$VDD - 0.4$	—	—	V
VOL	Digital I/O output logic low (ABZ , UVW , MISO , OUT)	Push-pull (@ Iout = 2 mA)	—	—	0.4	V
TRise	Rise Time	CL = 20 pF	—	—	50	ns
TFall	Fall Time	CL = 20 pF	—	—	50	ns

6 Applied Magnetic Field Parameters

Unless otherwise specified, the following parameters apply at supply voltage 3.0~5.5 V, temperature -40~125°C, with an externally applied 1-pole-pair radially magnetized cylindrical magnet.

Table 10: Applied Magnetic Field Parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
Dmag	Magnet Diameter	Recommended: 10 mm, 1-pole-pair radially magnetized	—	10	—	mm
Tmag	Magnet Thickness	Recommended magnet thickness 2.5 mm	—	2.5	—	mm
Bpk	Input magnetic field (horizontal direction parallel to chip surface)	Measured at chip surface	30	—	1,000	mT
AG	Air Gap	Distance from chip surface to magnet	—	1.0	3.0	mm
RS	Speed	—	—	—	60,000	RPM
DISP	Eccentricity	Offset of magnet center from chip sensing center	—	—	0.3	mm
TCmag1	Magnet Temperature Coefficient	NdFeB magnet	—	-0.12	—	%/°C
TCmag2	Magnet Temperature Coefficient	SmCo magnet	—	-0.035	—	%/°C

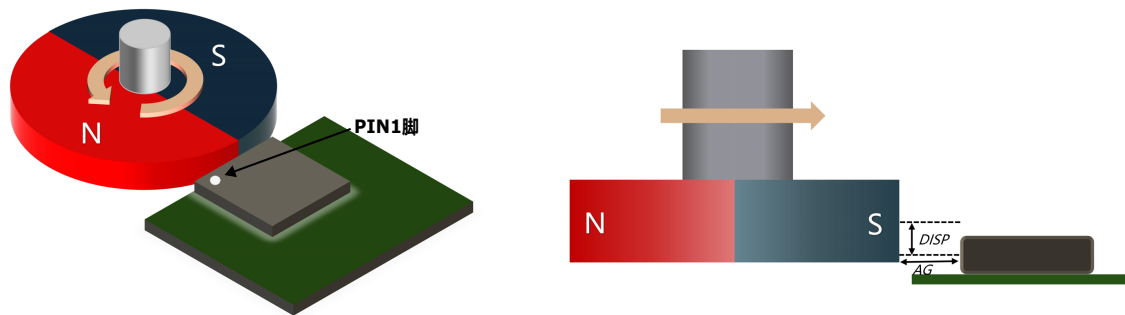


Figure 4: Magnet Eccentricity (DISP) and Air Gap (AG) Diagram

7 Output Interfaces and Modes

KTM5300 outputs ABZ, UVW, and PWM signals on the corresponding pins; 21-bit absolute angle data is read through dedicated 4-wire SPI pins.

7.1 I/O Pin Function Configuration

The ABZ single-ended/differential, UVW, PWM, and SPI interface pin configurations of KTM5300 are listed below. `IO_ORDER` is used to switch the output type of pins 1#~3#.

Table 11: I/O Pin Function Configuration (IO_ORDER)

Pin No.	IO_ORDER = 0	IO_ORDER = 1	Description
1	U	–A	UVW and differential ABZ shared
2	V	–B	UVW and differential ABZ shared
3	W	–Z	UVW and differential ABZ shared
5	MISO	MISO	SPI interface
6	MOSI	MOSI	SPI interface
7	SCK	SCK	SPI interface
8	CSN	CSN	SPI interface
10	OUT(PWM)	OUT(PWM)	PWM output
14	Z	Z	ABZ single-ended output
15	B	B	ABZ single-ended output
16	A	A	ABZ single-ended output

Table 12: CAL_EN Pin Trigger Behavior

Trigger Scenario	Typical Condition	Result
Nonlinear calibration trigger	Motor running steadily at a speed above the calibration start threshold	Calibration starts; whether the result is automatically written to MTP after completion is determined by <code>STORE_SEL</code>
Automatic zero-point setting trigger	Stationary or low-speed condition (speed $\leq$ 40 RPM)	Zero-point setting is performed automatically; result written to MTP per configuration; retained after power-down

Note: `CAL_EN` and SPI register triggers (such as `CAL_REG_SET` and `ZERO_SET`) can achieve similar functions, but their MTP write behaviors differ. A single trigger strategy should be fixed during mass-production configuration to avoid inconsistent parameter management from mixing both methods.

7.2 Reference Circuit

KTM5300 is powered from a single supply (3.3~5.0 V). It is recommended to place a decoupling capacitor of at least $0.1\mu\text{F}$ between the supply and ground pins, and to add a TVS diode in parallel to improve EMC performance. KTM5300 pin 4 (**CAL_EN**) and pin 13 (**TEST_EN**) have built-in $250\text{ k}\Omega$ pull-down resistors.

If customer-side self-calibration is required, refer to the recommended circuit shown below; the detailed procedure is described in the “Calibration” section.

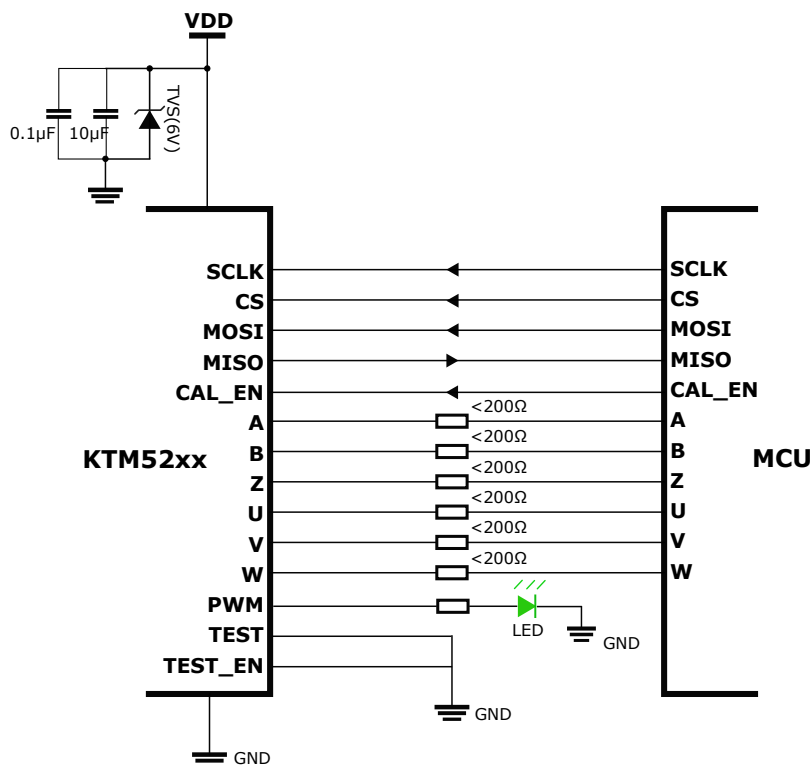


Figure 5: Reference Circuit (with Customer-Side Self-Calibration)

7.3 Quadrature A, B, and Zero-Position Z Signal Output (ABZ Mode)

When the magnet rotates counterclockwise (CCW, viewed from above the chip), the rising edge of **B** leads the rising edge of **A** by 1/4 of a period; when rotating clockwise (CW), the rising edge of **A** leads the rising edge of **B** by 1/4 of a period. The **Z** signal corresponds to the absolute 0° position. The chip does not output ABZ during the first 64 ms after power-up; after 64 ms it outputs a stable, valid ABZ signal.

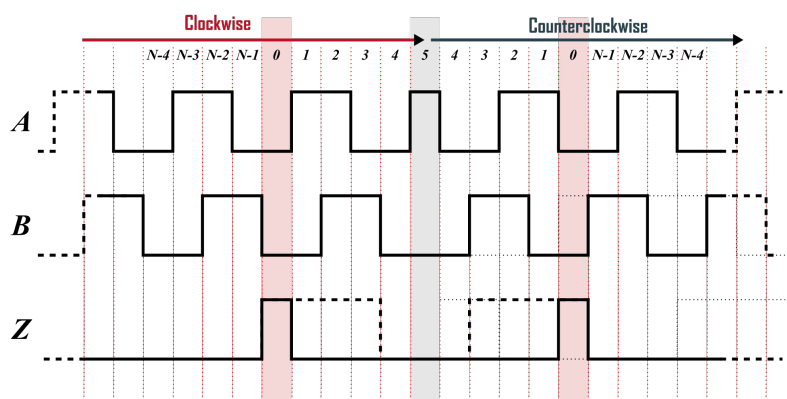


Figure 6: ABZ Output Mode

Table 13: ROT_DIR Rotation Direction Register

ROT_DIR	Rotation Direction
0	Magnet rotates CCW above the chip (viewed from above); B leads A , angle increases
1	Magnet rotates CW above the chip (viewed from above); A leads B , angle increases

ROT_DIR affects all angle outputs (ABZ, UVW, PWM, SPI).

KTM5300's ABZ output line count ranges from 1 to 65,536 lines/revolution, defined by the 16-bit register `ABZ_PPT[15:0]` (actual line count = `ABZ_PPT` + 1). Every 4 lines correspond to 1 pulse, giving an equivalent pulse range of 1~65,536 pulses/revolution. The correspondence between LSBs, steps/revolution, and pulses/revolution is shown in the figures below.

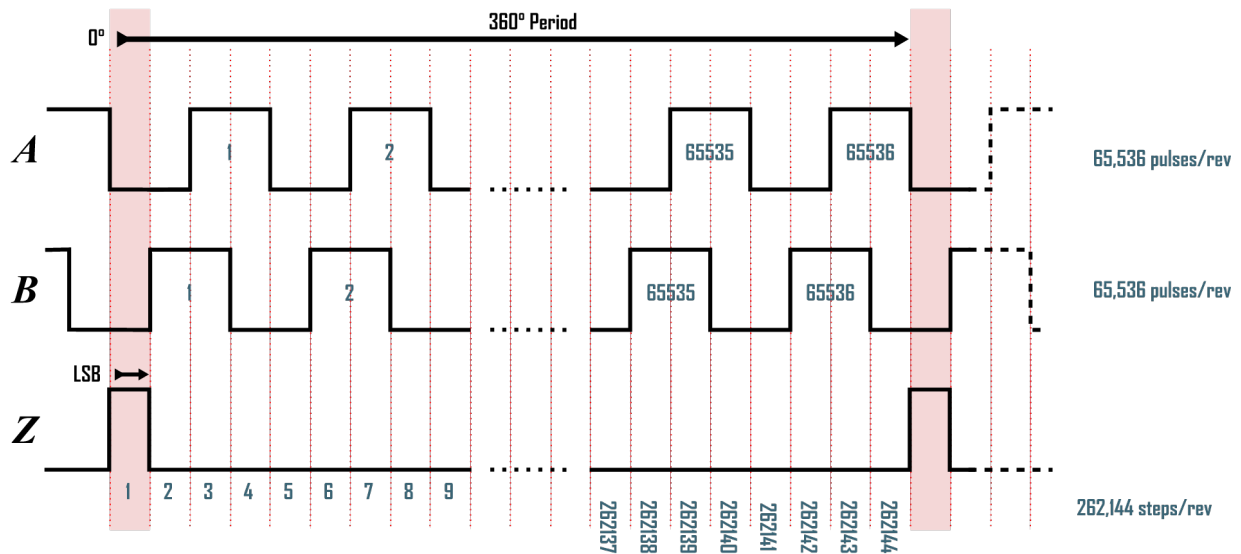


Figure 7: ABZ Output Resolution = 65,536 pulses/revolution

18-bit resolution = 2^{18} LSBs = 262,144 steps = 65,536 pulses.

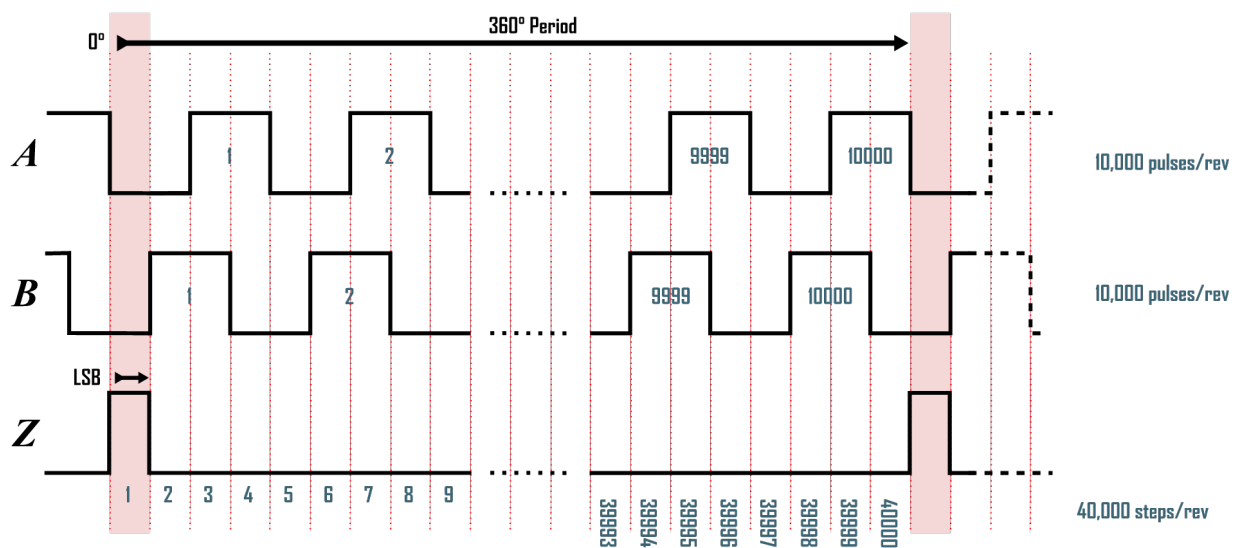


Figure 8: ABZ Output Resolution = 10,000 pulses/revolution

10,000 pulses = 40,000 steps. ABZ output resolution is defined by `ABZ_PPT[15:0]`, actual lines/rev = `ABZ_PPT + 1`, range 1~65,536:

Table 14: ABZ_PPT Resolution Register Truth Table

ABZ_PPT[15:0]	ABZ Lines (lines/rev)
0x0000	1
0x0001	2
0x0002	3
⋮	
0x3FFC	16,381
0x3FFD	16,382
0x3FFE	16,383
0x3FFF	16,384
⋮	
0xFFFE	65,535
0xFFFF	65,536

Table 15: ABZ_LIMIT[1:0] Frequency Limit Register Truth Table

ABZ_LIMIT[1:0]	AB Freq. Limit	Max Speed (RPM)	Condition
0x0	8.192 MHz	7,500	ABZ_PPT = 65535 (65,536 lines/rev, quadrature edge count)
0x1	4.096 MHz	3,750	Same as above
0x2	2.048 MHz	1,875	Same as above
0x3	1.024 MHz	937.5	Same as above

Table 16: ABZ_START Absolute-Position Start-up Output Behavior

ABZ_START	AB Output After Start-up	Freq. Limit	Description
0	Does not output absolute-position edges	Limited only by real-time speed	Chip enters normal incremental output after start-up
1	Re-issues AB edges per current absolute angle	Limited by ABZ_LIMIT	0°~180°: B leads A; 180°~360°: A leads B

Table 17: Z_EDGE Edge Alignment Definition

Z_EDGE	Alignment Behavior
0	Z rising edge is aligned with the absolute zero point (actual edge relationship determined together with AB phase)
1	Z falling edge is aligned with the absolute zero point (actual edge relationship determined together with AB phase)

The **z** signal indicates the absolute angular zero position. Its width is configurable to 1, 2, 4, 8, 16 LSBs, or 60°, 120°, or 180°. The **z** signal occurs only once per revolution.

The width of the Z signal is defined by the 3-bit register

Z_WIDTH[2:0]:

Table 18: Z_WIDTH Z-Signal Width Register Truth Table

Z_WIDTH[2:0]	Width (LSB or °)	Z_WIDTH[2:0]	Width (LSB or °)
0x0	1	0x4	16
0x1	2	0x5	60°
0x2	4	0x6	120°
0x3	8	0x7	180°

7.4 UVW Output Mode

KTM5300 provides UVW outputs spaced 120° apart, which can replace three switch-type Hall sensors for motor commutation control. The number of UVW pole pairs can be programmed in the range 1~64 pole pairs/revolution, defined by the 6-bit register UVW_PPT[5:0] (actual pole-pair count = UVW_PPT + 1). When IO_ORDER = 1, the UVW pins switch to differential ABZ output (–A/–B/–Z).

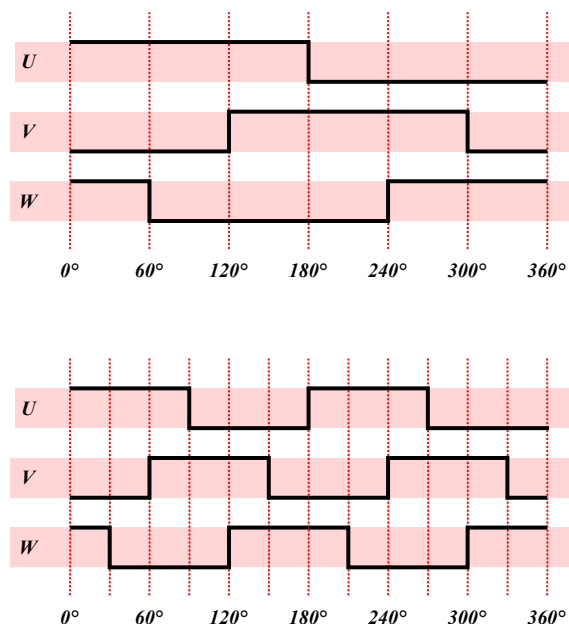


Figure 9: UVW Output Waveforms — Top: 1 pole pair, Bottom: 2 pole pairs

Table 19: UVW_PPT Pole-Pair Register Truth Table

UVW_PPT[5:0]	UVW Pole Pairs (pole pairs/rev)
0x00	1
0x01	2
0x02	3
⋮	
0x0F	16
⋮	
0x3F	64

Table 20: UVW and Z Edge Alignment Relationship

ROT_DIR	Z_EDGE	U-to-Z Alignment
0	0	U falling edge aligned with Z falling edge
0	1	U falling edge aligned with Z rising edge
1	0	U rising edge aligned with Z rising edge
1	1	U rising edge aligned with Z falling edge

7.5 SPI Interface

KTM5300 provides a 4-wire SPI interface that can be used to read the chip's internal 21-bit absolute angle data, configure registers, and program parameters into the built-in EEPROM.

7.5.1 SPI Timing Parameters

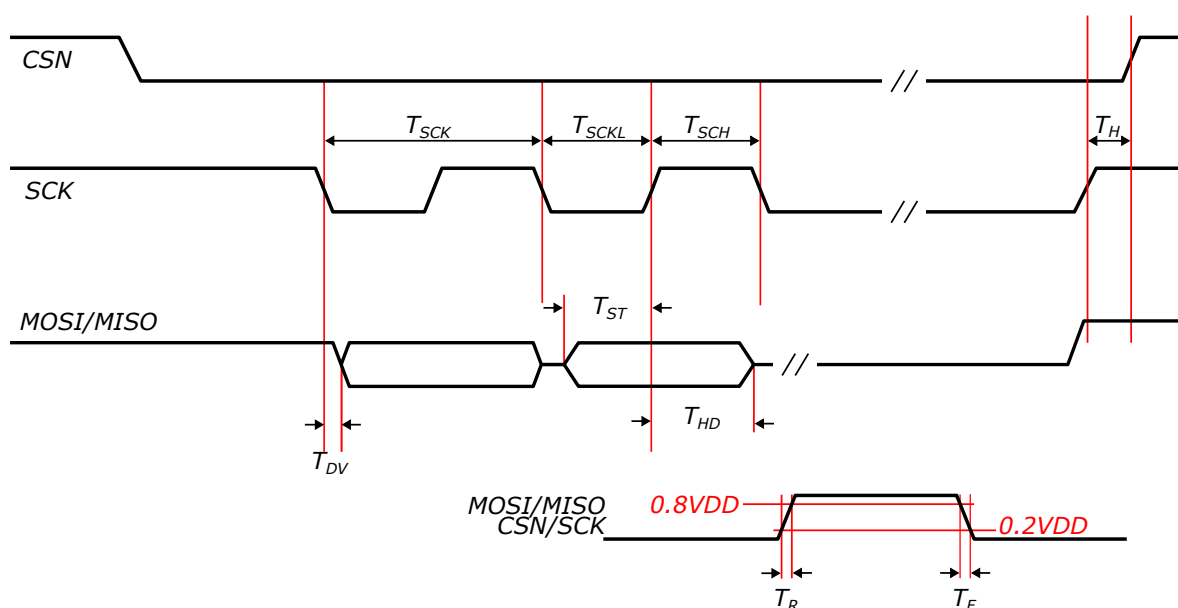


Figure 10: SPI Timing Diagram

The SPI timing diagram of KTM5300 is shown above. The table below lists the SPI timing parameters of KTM5300 under a 20 pF load condition. This table lists the symbol, description, and minimum, typical, and maximum values (in nanoseconds, ns) for each parameter.

Table 21: SPI Timing Parameters (20 pF Load Condition)

Symbol	Description	Min	Typ	Max	Unit
T_{SCK}	SCK clock period	50			ns
T_{SCKL}	SCK low period	25			ns
T_{SCKH}	SCK high period	25			ns
T_H	Time interval between SCK and CSN rising edges	12.5			ns
T_R	Rise time of digital signal		10		ns
T_F	Fall time of digital signal		10		ns
T_{DV}	MISO data valid (setup) time			15	ns
T_{ST}	MOSI data setup time	10			ns
T_{HD}	MOSI data hold time	10			ns

7.5.2 Basic SPI Parameters

KTM5300's SPI interface uses Mode 3 (CPOL=1, CPHA=1) with the following basic parameters:

- **SPI Mode:** Mode 3 (CPOL=1, CPHA=1)
- **SCLK Idle Level:** High
- **Data Switching/Sampling:** Data changes on SCLK falling edge; sampled on rising edge
- **Command Code Length:** 4 bits
- **Address Length:** 8 bits (for some commands)
- **Idle Field Length:** 4 bits (for some commands)
- **Data Length:** 8 bits (write or read)
- **CRC Length:** 8 bits (read operations and special commands only)
- **CRC Algorithm:** CRC-8, polynomial 0x07, initial value 0x00
- **CRC Output:** When $SPI_CRC = 1$, CRC result is XORed with 0xFF; when $SPI_CRC = 0$, CRC result is not XORed. Default value of SPI_CRC is 0.

7.5.3 SPI Command Formats

SPI command formats are as follows:

- **Read Register:** 0011 (host sends 4-bit command code + 8-bit register address + 4-bit idle)

- **Write Register:** 0110 (host sends 4-bit command code + 8-bit register address + 4-bit idle + 8-bit write data)
- **Special Command (read angle/status/CRC):** 1010 (host sends 4-bit command code + 12 bits of zeros)
- **Special Command (program MTP):** 1100 (host sends 4-bit command code + 12 bits of zeros)

7.5.4 Multiple SPI Slaves in Parallel

The figure below shows a reference circuit for multiple KTM5300 devices connected in parallel on the same SPI bus; the reference circuit for a single KTM5300 is shown earlier in this document.

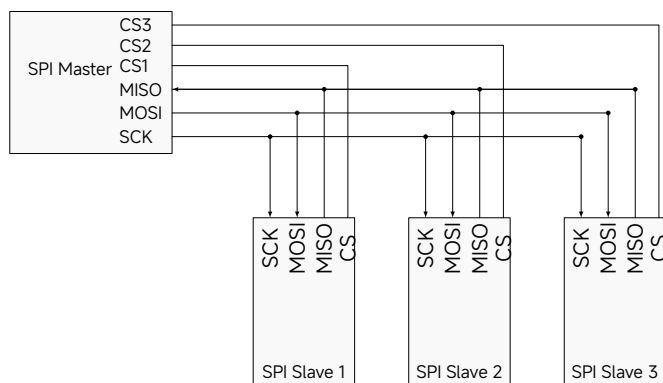


Figure 11: 4-Wire SPI Reference Circuit (Multiple Chips in Parallel)

7.5.5 Write Register Operation

Write register procedure:

1. Host pulls **CSN** low; SPI communication begins.
2. Host transmits on **MOSI** in sequence:
 - 4-bit command code (0110)
 - 8-bit register address
 - 4-bit idle field (typically 0)
 - 8-bit data to be written
3. The slave does not respond; **MISO** remains in high-impedance state.
4. Host pulls **CSN** high; communication ends.

Table 22: Write Register SPI Frame Format

Clock Cycle	MOSI Content	Description	MISO Content
1-4	0110	Command code	Z
5-12	Address	8-bit register address	Z
13-16	Idle	4-bit idle	Z
17-24	Data	8-bit write data	Z
25-	—	—	Z

Note: To prevent external interference from modifying internal registers, KTM5300 has a register-lock feature; registers cannot be written until unlocked. To unlock, write 0xAA to address 0x1A. After a successful unlock, reading register 0x1A returns 0x01. The chip automatically re-locks after a power cycle; no additional re-locking action is required.

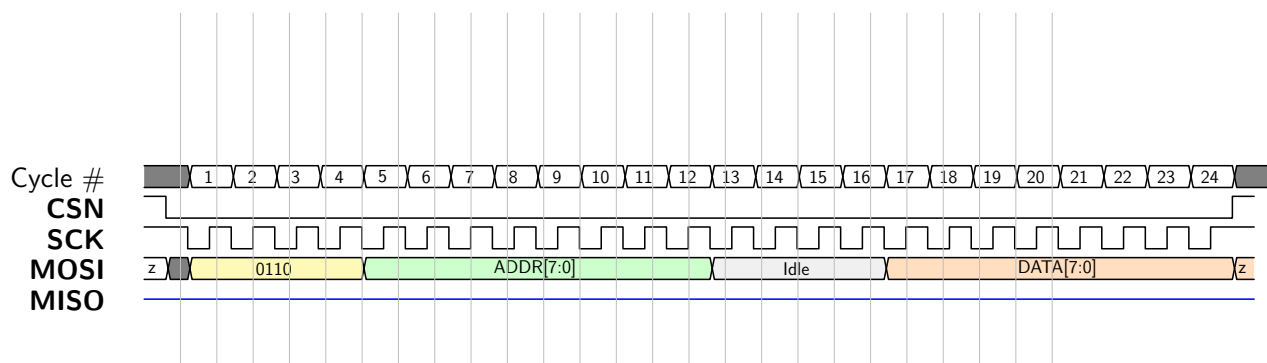


Figure 12: Write Register SPI Timing

7.5.6 Read Register Operation

Read register procedure:

1. Host pulls **CSN** low; SPI communication begins.
2. Host transmits on **MOSI** in sequence:
 - 4-bit command code (0011)
 - 8-bit register address
 - 4-bit idle field (typically 0)
3. Host continues to provide the clock; the slave's **MISO** switches from high-impedance to output:
 - 8 bits of register data
 - 8 bits of CRC check data
4. Host pulls **CSN** high; communication ends.

Table 23: Read Register SPI Frame Format

Clock Cycle	MOSI Content	Description	MISO Content
1-4	0011	Command code	z
5-12	Address	8-bit register address	z
13-16	Idle	4-bit idle	z
17-24	—	Host continues to provide clock	8-bit register data
25-32	—	Host continues to provide clock	8-bit CRC check data
33-	—	—	z

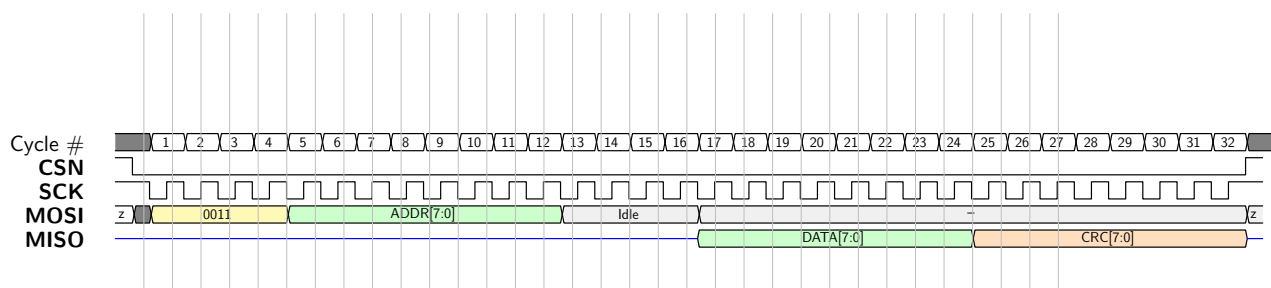


Figure 13: Read Register SPI Timing

7.5.7 Special Command: Read Angle/Status/CRC

Read angle/status/CRC procedure:

1. Host pulls **CSN** low; SPI communication begins.
2. Host transmits on **MOSI**: 4-bit command code (1010) followed by 12 bits of zeros (16 bits total).
3. Host continues to provide the clock; **MOSI** remains at 0 (or idle).
4. After the host has sent 16 bits, the slave's **MISO** switches from high-impedance to output, in sequence:
 - 21 bits of angle data (angle[20:0])
 - 3 bits of status data (status[2:0])
 - 8 bits of CRC check data (crc[7:0])
5. Continuing to provide **SCK** allows angle data to be output continuously.
6. Host pulls **CSN** high; communication ends.

Table 24: status[2:0] Status Bit Description

Status Bit	Description (active high)
status[0]	Overspeed warning, or memory CRC check failure
status[1]	ADC amplitude warning
status[2]	Chip supply under-voltage warning

Table 25: Read Angle/Status/CRC SPI Frame Format

Clock Cycle	MOSI Content	Description	MISO Content
1-4	1010	Command code	z
5-16	0	Placeholder/idle	z
17-37	0	Placeholder/idle	angle[20:0]
38-40	0	Placeholder/idle	status[2:0]
41-48	0	Placeholder/idle	crc[7:0]
49-	0	Placeholder/idle	z

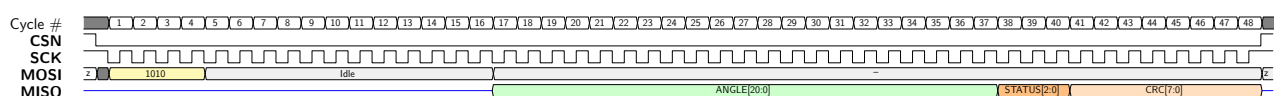


Figure 14: Angle Read SPI Timing

7.5.8 Special Command: Program MTP

Program MTP procedure:

1. Host pulls **CSN** low; SPI communication begins.
2. Host transmits on **MOSI**:
 - 4-bit command code (1100)
 - 12 bits of zeros (placeholder/idle; no address or data)
3. Host continues to provide the clock; after the slave receives the complete command, **MISO** switches from high-impedance to output and replies with 0x55 (01010101).
4. Host pulls **CSN** high; communication ends.
5. Wait at least 2.5 s for MTP programming to complete; powering down early may corrupt register contents.

Table 26: Program MTP SPI Frame Format

Clock Cycle	MOSI Content	Description	MISO Content
1-4	1100	Command code	z
5-16	0	12 bits of zeros	z
17-24	—	Host continues to provide clock	0x55 (01010101)
25-	—	—	z

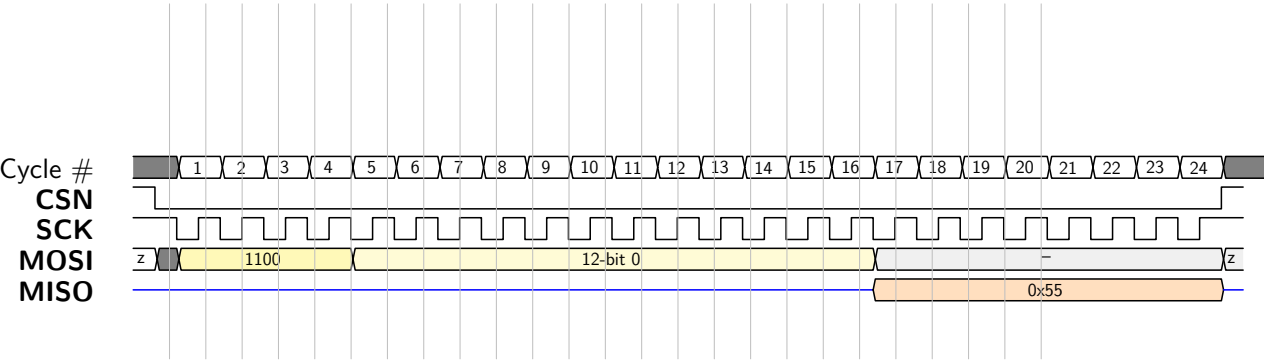


Figure 15: Program MTP SPI Timing

8 Zero-Point Setting and Parameter Storage

The zero-point position register `ZERO[20:0]` of KTM5300 defines the 0° position of the output angle data; it is 21 bits wide. There are three methods for setting the zero point:

Table 27: ZERO[20:0] Zero-Point Register

Address	Register	Type
0x4B	ZERO[7:0]	E
0x4C	ZERO[15:8]	E
0x4D	RESERVE ZERO[20:16]	E

Table 28: Comparison of Three Zero-Point Setting Methods

Method	Trigger	Write MTP	Condition / Remarks
SPI write zero-point register	Write directly to <code>ZERO[20:0]</code>	No	Takes effect immediately; an additional MTP program command is required for persistent storage
Write <code>ZERO_SET</code>	Write 1 to <code>ZERO_SET</code> ; chip automatically writes current angle to <code>ZERO[20:0]</code>	No	Suitable for software zeroing
<code>CAL_EN</code> pin	Assert <code>CAL_EN</code> high while stationary (speed $\leq$ 40 RPM)	Yes	Automatically programs MTP addresses 0x00~0x0F; affected by <code>CAL_DEGLITCH</code> and <code>ZERO_PIN_DIS</code>

Note: Method 1 (SPI register write) and Method 2 (`ZERO_SET`) do NOT write `ZERO[20:0]` to MTP; the zero-point setting is lost after a power cycle. To save permanently, an additional MTP program command must be executed. Method 3 (`CAL_EN` pin) automatically writes to MTP; the zero point is retained after power cycling.

8.1 Auto Zero-Point Setting via SPI `ZERO_SET`

After adjusting the system to the target 0° physical position, write 1 to `ZERO_SET` via the SPI write-register command. The chip automatically writes the current angle to `ZERO[20:0]`; `ZERO_SET` clears automatically when the operation is complete.

8.2 Manual Calculation and SPI Write to ZERO[20:0]

- (a) First, clear ZERO[20:0] to zero via SPI (write 0, to avoid interfering with the calculation);
- (b) Read the current angle register data via SPI (or use the 1010 command to read the angle);
- (c) Calculate the target zero-point value and write it to ZERO[20:0] via the SPI write-register command.

For either of the above two methods, if the zero-point data must be permanently saved, an additional MTP program command must be executed.

8.3 Zero-Point Function Behavior

The behavior of direct ZERO[20:0] write, ZERO_SET zeroing, and CAL_EN pin zeroing is as follows.

Table 29: Zero-Point Function Behavior

Method	Trigger Register / Pin	Auto Write MTP	Description
Manual zero write	ZERO[20:0]	No	Angle zero takes effect immediately; lost after power-down; requires manual MTP programming to retain
Software auto zero	ZERO_SET	No	Write 1 to automatically capture current angle and zero it; ZERO_SET clears automatically when done
Pin zero	CAL_EN	Yes	Reliably triggered at standstill or low speed; automatically executes zeroing and writes to MTP per configuration

9 Calibration

KTM5300 provides a customer-side calibration mechanism to ensure accuracy after physical installation. The calibration process consists of two core stages: linear calibration (compensating AMR signal amplitude/quadrature errors) and nonlinear calibration (eliminating higher-order nonlinear errors).

9.1 Linear Calibration

Linear calibration operates as an **online iterative** process. While the system rotates, parameters are automatically updated at each zero crossing. This allows the calibration to automatically compensate for amplitude, offset, and phase errors of the front-end analog signals.

Table 30: Linear Calibration Key Registers

Register Name	Width	Type	Function
LNR1_EN	1	E	Enable stage-1 linear calibration
LNR2_EN	1	E	Enable stage-2 linear calibration
LNR1_UPD	1	E	Trigger stage-1 linear parameter iteration
LNR2_UPD	1	E	Trigger stage-2 linear parameter iteration

9.2 Nonlinear Calibration

Nonlinear calibration uses a **64-point Golden lookup table** (register addresses 0x80~0xFF, 128 bytes total) to compensate for higher-order nonlinear errors. The chip divides 360° into 64 equal sectors; each sector corresponds to a 16-bit Golden angle value. After a table lookup, the final angle output is computed via Bezier interpolation.

The Golden table can be obtained by two methods:

- **Nonlinear self-calibration:** While the system rotates steadily, the on-chip algorithm automatically computes and updates the Golden table without external reference equipment.
- **Nonlinear back-to-back calibration:** Run this chip against a high-accuracy reference encoder; the host computes the error and writes the corrected Golden values directly to 0x80~0xFF for higher accuracy.

Both methods write to the same Golden table (0x80~0xFF) and can overwrite each other.

9.2.1 Nonlinear Self-Calibration

Nonlinear self-calibration uses the on-chip algorithm to automatically learn nonlinear errors during operation and update the Golden table in real time. Two calibration modes are supported (controlled by `ANLC_MODE`):

Table 31: ANLC_MODE Calibration Mode Comparison

ANLC_MODE	Mode	Characteristics
0	Slow Mode	Longer calibration time (~60 s at 800 RPM); higher accuracy; stronger noise immunity
1	Fast Mode	Short calibration time (~15 s at 200 RPM); fast convergence; suitable for low-noise conditions

Procedure:

(1) Configure the calibration mode: set `ANLC_MODE` via SPI to select slow or fast mode.

(2) Run the system steadily at the target speed (recommended above the calibration start threshold of 40 RPM; maintain stable speed).

(3) Trigger self-calibration by either of the following methods:

- **Register trigger:** Write 1 to `CAL_REG_SET` (address 0x17) to start calibration; write 0 to stop.
- **Pin trigger:** Pull the `CAL_EN` pin from low to high; maintain high level for longer than the debounce time configured by `CAL_DEGLITCH`.

(4) Maintain the current speed until calibration succeeds. During this period, the PWM pin (pin 10) outputs a calibration-status square wave: ~3.8 Hz when `PWM_FQ` = 0, ~1.9 Hz when `PWM_FQ` = 1. The calibration status can be monitored in real time by the duty cycle:

Table 32: Self-Calibration Status (PWM Output Indication and ANLC_STATUS)

ANLC_STATUS	Calibration State	PWM Frequency	PWM Duty Cycle
0	Not calibrated	Normal operating frequency	Position or speed information
1	Calibrating	PWM_FQ=0: ~3.8 Hz; PWM_FQ=1: ~1.9 Hz	50%
2	Calibration failed	PWM_FQ=0: ~3.8 Hz; PWM_FQ=1: ~1.9 Hz	$\approx 0\%$ ($1/2^{17}$)
3	Calibration successful	PWM_FQ=0: ~3.8 Hz; PWM_FQ=1: ~1.9 Hz	$\approx 100\%$ ($1 - 1/2^{17}$)

The calibration status can also be read via SPI register ANLC_STATUS[1:0] (address 0x16).

(5) If calibration fails, check whether the speed is within the configured range and sufficiently stable, then re-trigger calibration.

(6) After successful calibration, to permanently save the Golden table:

- **Pin-triggered mode:** Confirm STORE_SEL = 1; the table is automatically written to MTP after calibration completes.
- **Register-triggered mode:** After calibration completes, manually execute the MTP program command (command code 1100).

(7) After MTP programming is complete, power cycle the chip before proceeding with other operations.

Table 33: Nonlinear Self-Calibration Key Registers

Register Name	Width	Type	Function
NLNR_EN	1	E	Nonlinear calibration enable (= 0: bypass the entire module)
CAL_REG_SET	1	D	Register-triggered calibration (write 1 to start; write 0 to stop)

9.2.2 Nonlinear Back-to-Back Calibration

Nonlinear back-to-back calibration uses an external high-accuracy reference to compute angle errors; accuracy is typically better than self-calibration. The recommended

setup uses two coupled servo systems where the master motor carries a high-accuracy optical encoder as the reference angle source.

Calibration principle: Compare the chip output angle against the reference encoder point by point; compute the Golden correction value for each sector. Write the results to 0x80~0xFF via SPI write-register commands and program to MTP for permanent storage.

Procedure:

- (1) Set `NLNR_EN` to 0 to temporarily disable nonlinear calibration; use raw angle data for sampling.
- (2) Run the back-to-back system at constant speed; the host simultaneously collects the chip output angle (SPI 1010 command) and the reference encoder angle.
- (3) Sample a sufficient number of revolutions uniformly over 360°; compute the Golden angle correction value for each of the 64 sectors.
- (4) Write the 64 Golden values (each 16 bits) to 0x80~0xFF via SPI write-register commands.
- (5) Set `NLNR_EN` to 1 to enable nonlinear calibration; verify the post-calibration accuracy.
- (6) Once accuracy meets requirements, execute the MTP program command (command code 1100) to permanently save the Golden table.
- (7) Power cycle and verify the calibration result.

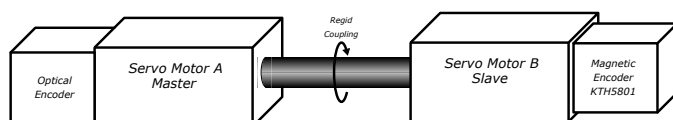


Figure 16: Recommended Nonlinear Back-to-Back Calibration Setup

Golden table format: `GLD_0~GLD_63` are 16-bit unsigned integers stored at 0x80~0xFF (low byte at lower address). The default values form a uniform linear distribution:

$$GLD_N = n \times \frac{2^{16}}{64} = n \times 0x0400 \quad (n = 0, 1, \dots, 63)$$

Both nonlinear calibration methods write to the same Golden table and can overwrite each other; the last content programmed to MTP takes effect.

9.2.3 EEPROM Write Behavior

The EEPROM write regions for zero-point and calibration operations under different trigger modes are shown below. Before writing, the register lock must be released: write 0xAA to address 0x1A to activate REG_WRITE_UNLOCK[7:0].

Table 34: Zero-Point Trigger and EEPROM Write Region

Trigger Method	Key Register / Pin	EEPROM Write Region	Remarks
Register-triggered zero	ZERO[20:0] / ZERO_SET	–	Modifies RAM registers only; not automatically flushed to MTP
Pin-triggered zero	CAL_EN	0x40~0x4F	Automatically written to MTP after zeroing

Table 35: Calibration Trigger and EEPROM Write Region

Calibration Trigger	EEPROM Write Region	Remarks
Register trigger	0x60~0xFF	Automatically saved after successful calibration
Pin trigger	0x60~0xFF	Automatically saved after successful calibration

10 Register Table

10.1 Read/Write Attribute Description

Table 36: Register Read/Write Attributes

Attr.	Full Name	Description
E	EEPROM	Readable and writable; data stored in EEPROM, retained after power-down
D	Dynamic	Readable and writable; data stored in register, lost after power-down
R	Read-only	Read-only; typically status or monitoring registers

Note: After power-up the registers are locked by default. You must write 0xAA to address 0x1A (the password register) to unlock before performing write operations on E/D type registers.

10.2 Complete Register Table

The “Default” column shows the chip power-on default register value; “—” indicates a read-only or chip-internally determined value.

Table 37: Full Register Table (KTM5300)

Address	Register	Type	Default
BLK0 Status/Control Registers (0x0C~0x1A)			
0x0C	PRODUCT_ID[7:0]	R	—
0x12	RESERVE ZERO_SET	D	0x00
0x13	DIFF_AVG[7:0]	R	—
0x14	DIFF_AVG[15:8]	R	—
0x15	DIFF_AVG[23:16]	R	—
0x16	RESERVE ANLC_STATUS[1:0]	R	—
0x17	RESERVE CAL_REG_SET	D	0x00
0x1A	REG_WRITE_UNLOCK[7:0]	D	0x00
BLK1 Function Configuration Registers (0x4B~0x6B)			
0x4B	ZERO[7:0]	E	0x00
0x4C	ZERO[15:8]	E	0x00

(Continued on next page)

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Address	Register								Type	Default
	7	6	5	4	3	2	1	0		
0x4D	RESERVE			ZERO[20:16]					E	0x00
	7	6	5	4	3	2	1	0		
0x51	ROT_DIR	RESERVE	NLNR_EN	RESERVE					E	0x7B
	7	6	5	4	3	2	1	0		
0x52	LNR2_UPD	LNR1_UPD	LNR2_EN	LNR1_EN	PWM_POL	PWM_SRC	PWM_FQ	PWM_EN	E	0x01
	7	6	5	4	3	2	1	0		
0x54	FILTER[7:0]								E	0x66
	7	6	5	4	3	2	1	0		
0x55	MAG_TH[7:0]								E	0x30
	7	6	5	4	3	2	1	0		
0x56	HYST[7:0]								E	0x08
	7	6	5	4	3	2	1	0		
0x57	ABZ_LIMIT[1:0]		ABZ_PHASE[1:0]		Z_EDGE	Z_WIDTH[2:0]			E	0x01
	7	6	5	4	3	2	1	0		
0x58	RESERVE			WEAK_MAG	RESERVE	ABZ_START	ABZ_DIR	ABZ_EN	E	0x01
	7	6	5	4	3	2	1	0		
0x59	ABZ_PPT[7:0]								E	0xFF
	7	6	5	4	3	2	1	0		
0x5A	ABZ_PPT[15:8]								E	0x7F
	7	6	5	4	3	2	1	0		
0x5B	UVW_PPT[5:0]						IO_ORDER	UVW_EN	E	0x21
	7	6	5	4	3	2	1	0		
0x68	DEVICE_ID[7:0]								E	0x00
	7	6	5	4	3	2	1	0		
0x69	DEVICE_ID[15:8]								E	0x00
	7	6	5	4	3	2	1	0		
0x6A	DEVICE_ID[23:16]								E	0x00
	7	6	5	4	3	2	1	0		
0x6B	DEVICE_ID[31:24]								E	0x00
	7	6	5	4	3	2	1	0		
Nonlinear Calibration Golden Table (0x80~0xFF)										
0x80+2N	GLD_N[7:0]								E	0x00
	7	6	5	4	3	2	1	0		
0x81+2N	GLD_N[15:8]								E	0x04×N
	7	6	5	4	3	2	1	0		
0x80	GLD_0[7:0]								E	0x00
	7	6	5	4	3	2	1	0		
0x81	GLD_0[15:8]								E	0x00
	7	6	5	4	3	2	1	0		
0xFE	GLD_63[7:0]								E	0x00
	7	6	5	4	3	2	1	0		
0xFF	GLD_63[15:8]								E	0xFC
	7	6	5	4	3	2	1	0		

Note: Do not arbitrarily modify register bits marked as RESERVED; doing so may cause the chip to enter an unrecoverable state.

After power-on reset, the nonlinear calibration Golden table (addresses 0x80~0xFF, 64 16-bit parameters) defaults to a **uniform linear distribution** as the initial reference for the nonlinear compensation curve. The high byte GLD_N[15:8] (at odd addresses) increments from 0x00 in steps of 0x04 up to 0xFC (i.e., $GLD_N[15:8] = 0x04 \times N$, $N = 0 \dots 63$);

the low byte `GLD_N[7:0]` (at even addresses) is `0x00` throughout. After nonlinear self-calibration, the chip writes compensation data to this region and stores it to MTP.

10.3 Register Descriptions

(1) 0x12~0x1A Status/Control Registers

- `ZERO_SET`: Software zeroing trigger bit. Writing 1 causes the chip to immediately map the current mechanical angle to the electrical angle zero point; the bit clears automatically when the operation is complete. Suitable for online zeroing or quick calibration after assembly.
- `ANLC_STATUS[1:0]`: Nonlinear calibration status read-only field. Use this to determine whether the calibration process has completed and whether it succeeded. Poll this field periodically after triggering calibration; implement a timeout mechanism to handle anomalies.
- `CAL_REG_SET`: Register calibration trigger control bit. Write 1 to enter the calibration process; write 0 to exit. Use this instead of the pin-triggered method to achieve pure SPI control.
- `CRC_ERR`: SPI communication CRC error flag (read-only). When this bit is set, the most recent transaction contained a checksum error; handle it in combination with the host retransmission strategy and link integrity checks.
- `REG_WRITE_UNLOCK[7:0]`: Write-protection unlock password register. Writing `0xAA` allows subsequent writes to E/D type registers. It is recommended to execute an unlock before each batch of critical parameter writes, then immediately read back to confirm.

(2) 0x4B~0x4F Zero-Point Configuration Registers

- `ZERO[7:0]`, `ZERO[15:8]`, `ZERO[20:16]`: 21-bit zero-point offset. These parameters determine the phase reference of the electrical angle output relative to the mechanical angle; commonly used for zero alignment after complete machine assembly.

(3) 0x50~0x52 SPI and Output Path Registers

- `ROT_DIR`: Rotation direction definition (CW/CCW). Used to align the mechanical direction with the

electrical angle output direction; prevents system-level direction inversion.

- **NLNR_EN**: Nonlinear calibration enable; set to 1 to enable.
- **LNR1_EN, LNR2_EN**: Stage-1/stage-2 linear compensation enable bits. Enable compensation functionality in stages to facilitate step-by-step evaluation of compensation effectiveness.
- **LNR1_UPD, LNR2_UPD**: Linear compensation parameter update control bits. Trigger new parameter activation; it is recommended to update uniformly after writing all parameters.
- **PWM_EN, PWM_FQ, PWM_SRC, PWM_POL**: PWM output enable, frame frequency, data source, and polarity configuration; for interfacing with different MCU capture chains.

(4) 0x54~0x5B ABZ/UVW and Diagnostic Registers

- **FILTER[7:0]**: Filter depth.
- **MAG_TH[7:0]**: Magnetic field strength decision threshold. Configure based on actual measured magnetic circuit amplitude to balance sensitivity and false-alarm rate.
- **HYST[7:0]**: Output hysteresis. Suppresses high-frequency toggling caused by boundary jitter; especially applicable near low-speed standstill conditions.
- **ABZ_LIMIT[1:0]**: AB-phase output frequency upper-limit configuration (8.192/4.096/2.048/1.024 MHz).
- **ABZ_PHASE[1:0]**: Z-phase position selection bits; used to align with the system reference zero position.
- **Z_EDGE, Z_WIDTH[2:0]**: Z-pulse active edge and width configuration; for compatibility with different drive controller Z-pulse definitions.
- **ABZ_EN, ABZ_DIR, ABZ_START**: ABZ output enable, direction, and startup absolute-position re-issue control bits.
- **INTER_DIS, WEAK_MAG, LNR_THD[2:0]**: Interpolation-disable, weak-field diagnostic, and linearity-threshold control bits; used to improve stability under abnormal magnetic field conditions.

- `ABZ_PPT[15:0]`: ABZ pulses per revolution setting (actual pulses/rev = register value + 1); determines encoder resolution and speed-feedback granularity.
- `UVW_PPT[5:0]`, `IO_ORDER`, `UVW_EN`: UVW pole-pair count, phase order, and output enable; used to match the motor pole-pair count and drive controller phase sequence.

(5) 0x80~0xFF Nonlinear Golden Table Registers

- `GLD_0~GLD_63`: Nonlinear compensation Golden table, comprising 64 16-bit node parameters. Parameters are organized in low-byte-at-lower-address / high-byte-at-higher-address order. The calibration algorithm corrects the full-angle error curve based on this table.

11 Package Information

KTM5300 is available in a QFN16L-3×3 package (16 pins), suitable for off-axis installation. The package outline drawing and dimensional specifications are shown below.

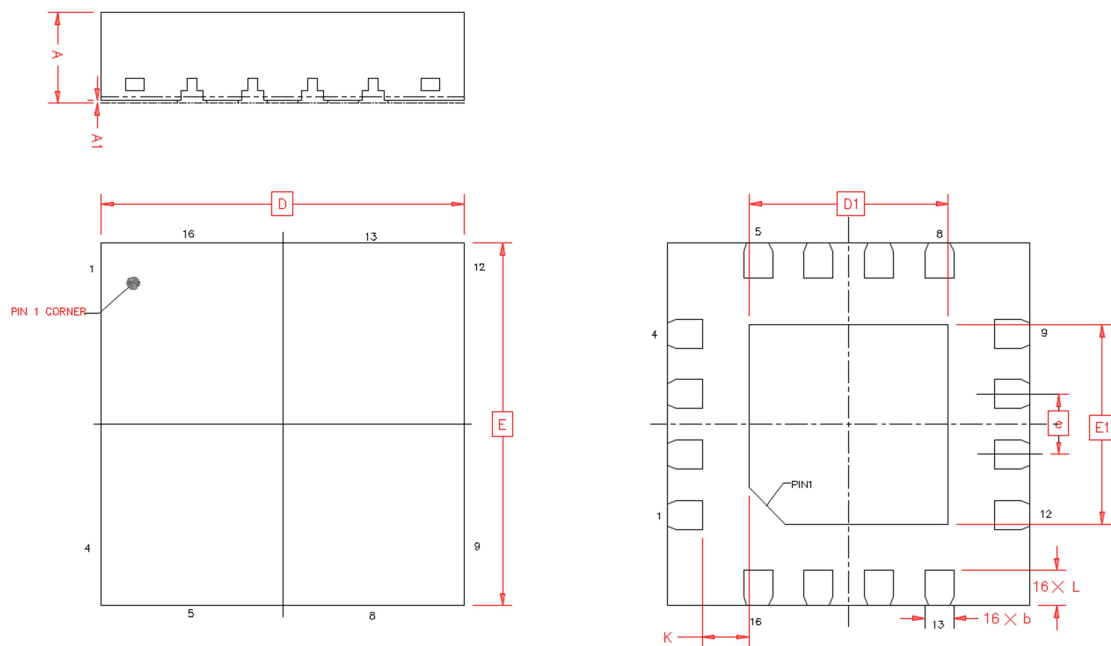


Figure 17: QFN-16L Package Outline

Note:

- The shape and quantity of exposed metal on the package sides may vary.
- No side-wettable flank design.

Table 38: QFN16L-3×3 Package Dimensions (Unit: mm)

Symbol	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.203 (REF)	—
D		3.000 (BSC)	
E		3.000 (BSC)	
D1	1.500	1.650	1.800
E1	1.500	1.650	1.800
k		0.385 (BSC)	
b	0.180	0.240	0.300
e		0.500 (BSC)	
L	0.190	0.290	0.390

Tape and Reel Dimensions

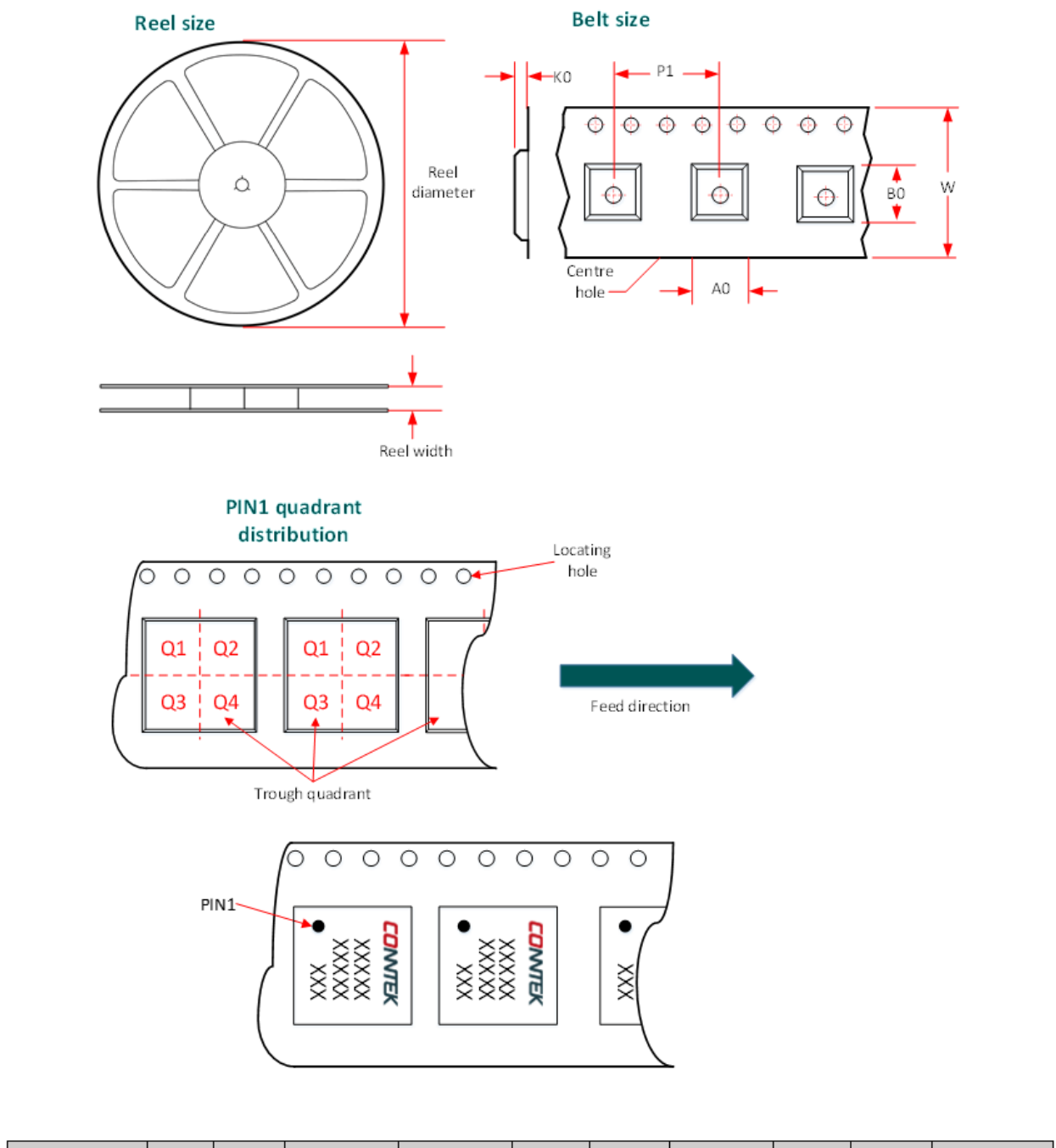


Figure 18: QFN-16L Tape and Reel

Table 39: QFN16L-3×3 Tape and Reel Dimensions

Package	Pins	SPQ	Reel Dia.	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Dir.
QFN16L-3×3	16	5000	330	12.4	3.35	3.35	1.13	8.00	12.00	Q1

Ordering Information

Table 40: Ordering Information

Part Number	Mount Type	Package	Packaging
KTM5300-QN16	Off-Axis	QFN16L-3×3	Tape and Reel (5000 pcs/reel)

- QFN3X3 package is a Moisture Sensitivity Level 3 (MSL-3) device.